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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WAI, ERIC CHARLES	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,944	BOUDON ET AL.	
	Examiner	Art Unit	
	ERIC C. WAI	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2-6 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 2-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 2 lines 11-13 recite, that the task management circuit is "configured to store a valid task being presented to all of said storage fields in parallel on said dedicated bus". This is contrary that what is enabled by the specification. [0026] of the specification indicates that the task is presented in parallel to the memory fields, but it is only loaded at the first field for which the valid bit is set to zero. The plain meaning of the above limitation of claim 2 implies that the valid task is *stored* in parallel to all of the storage fields when presented.

Claim 2 lines 15-16 recite, "enable said writing in the first free field below the pile". This is contrary to the plain meaning of FIFO (First In First Out) memory which only allows writing to the top of the FIFO (i.e. First In).

Claims 3-6 are directly or indirectly dependent upon claim 2 and do not remedy the issues above. Therefore, they are also rejected for the reasons given above.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms are not clearly understood:

i. Claim 2 lines 5-6 recite, “a first logic means for enabling *valid* tasks having an address *useful* for at least one slave device". It is unclear whether the task is enabled as a valid task if that task has a useful address for a slave device, or whether all tasks have an address useful for at least one slave device (i.e. is there a relationship between a valid task and having a useful address?).

ii. Claim 2 line 6 recites, “followed by corresponding data”. It is unclear what is meant by followed by corresponding data (i.e. where is the data located? Inside the task? At the address? At the slave device?).

iii. Claim 2 line 7 recites, “a dedicated bus”. It is unclear whether this is the same as the processor bus in line 2.

iv. Claim 2 line 9 recites, "comprising a FIFO memory". It is unclear if this is the same or different from the FIFO memory of line 2.

v. Claim 2 line 10 recites, "provided with a plurality of N Storage fields forming a pile". It is unclear what component is provided with the storage fields (i.e. task management circuit, FIFO memory, dedicated bus?).

vi. Claim 2 line 18 recites, "a FIFO controller". It is unclear whether this is the same or different from line 1.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Kawahara (US Pat No. 6,246,257) further in view of Callander et al. (US Pat No. 5,579,504).

8. Regarding claim 2, AAPA teaches a FIFO based controller for slave devices attached to a processor bus of a CPU for processing tasks and storing the tasks in a FIFO memory, wherein a task consists of an address and its associated qualifying bits ([0004] lines 3-9) , the improved FIFO based controller comprising:

a first logic means for enabling valid tasks, having an address useful for at least one slave device, followed by corresponding data and for inhibiting others to be presented on a dedicated bus ([0004] lines 3-9);

a task management circuit coupled to said first logic means, said task management circuit comprising a FIFO memory connected to said dedicated bus and provided with a plurality of N storage fields forming a pile, each field being identified by a determined address and configured to store a valid task being presented (it is inherent that a FIFO based controller would have a FIFO memory with N storage fields to store task information for the slave devices).

9. However, AAPA does not teach that the FIFO memory is configured to store a valid task being presented to all of said storage fields in parallel on said dedicated bus. Kawahara teaches a technique allowing for parallel access to a FIFO having multiple input and output ports (col 3 lines 2-5).

10. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the conventional controller circuits of AAPA to utilize Kawahara's invention. One would be motivated by the desire to increase efficiency by allowing simultaneous access as taught by Kawahara (col 1 lines 18-23).

11. AAPA and Kawahara do not teach a second logic means that inhibit the writing of a task in the field(s) of the FIFO memory where a valid task has been entered and enable said writing in the first free field below in the pile.

12. It is well known in the art that FIFO memory is first in first out memory, where items are added to the memory in a queuing fashion. Callander teaches one such FIFO queue containing multiple entries, where each entry has a data field and a valid bit (col 3 lines 18-20). Incoming data is placed on one end of the queue and valid bits are set for those entries (col 3 lines 20-27). Valid bits are cleared for entries taken off the other end of the queue (col 3 lines 27-29).

13. It would have been obvious to one of ordinary skill in the art to inhibit the writing of tasks to a field where a valid task has been entered and writing the task to first free field below since operation of a FIFO memory occurs in such a fashion. One would be motivated by the desire to not overwrite valid entries such as taught by Callander.

14. AAPA, Kawahara, and Callander do not explicitly teach that the first logic means comprises: a task detection circuit coupled to the processor bus that detects valid tasks; and, a FIFO controller coupled to said task detection circuit, said FIFO controller generates an ADD TASK signal to add new tasks to be performed in said FIFO memory, a CLEAR TASK signal that clears all tasks therefrom that have been executed when said corresponding data are available on the processor bus, and a control signal that is applied to a gating means for only enabling said valid tasks to be presented on said dedicated bus.

15. Callander does however teach adding new entries to FIFO queue and setting valid bits for those entries (col 3 lines 20-27) and clearing valid bits for entries that are removed from the other end of the queue (col 3 lines 27-29).

16. It would have been obvious to one or ordinary skill in the art at the time of the invention to include a signal to add and remove tasks from the FIFO memory. One would be motivated by the desire to signal the addition and removal of tasks for processing such as taught by Callander.

17. Regarding claim 3, Callander teaches a valid bit (V) stored in a register is associated to each of said N storage fields, wherein a first binary value being set in said register, means that a valid task has been entered in the corresponding field (col 3 lines 17-20).

18. Regarding claim 5, Kawahara teaches that said second logic means enables said writing in all the free fields of the FIFO memory instead of only the first free field (col 2 lines 7-12, wherein any field can be accessed in RAM).

19. Regarding claim 6, AAPA teaches the use of multiple slave devices ([0003-4]), but does not teach a slave controller coupled to said processor bus and task management circuit. It would have been obvious to one or ordinary skill in the art at the time of the invention to couple a slave controller to the processor bus and task management circuit. It is well known in the art that slave controllers are widely used in computer processing systems.

20. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA), Kawahara (US Pat No. 6,246,257), and Callander et al. (US Pat No. 5,579,504), further in view of Hamlin Jr. et al (US Pat No. 5,157,655).

21. Regarding claim 4, AAPA, Kawahara, and Callander do not teach that the output of each pair of consecutive registers is connected to the inputs of a two-way XOR gate, so that only one output of the N-1 XOR gates is active (at "1") indicating thereby the boundary between the field(s) of the FIFO memory where a valid task has been entered and the remaining free field(s).

22. Hamlin teaches a method of using an XOR gate for comparing the most significant bits for providing an indication of the fullness of a FIFO (col 7 lines 6-8).

23. It would have been obvious to one or ordinary skill in the art at the time of the invention to connect the output of the registers to a two-way XOR gate. It is well known in the art the XOR gate is a commonly used component in logic.

Response to Arguments

24. Applicant's arguments with respect to claims 2-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC C. WAI whose telephone number is (571)270-1012. The examiner can normally be reached on Mon-Fri, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Eric C Wai/
Examiner, Art Unit 2195